

EDITED BY BILL TRAVIS &amp; ANNE WATSON SWAGER

# Demodulator makes low-cost optical tracker

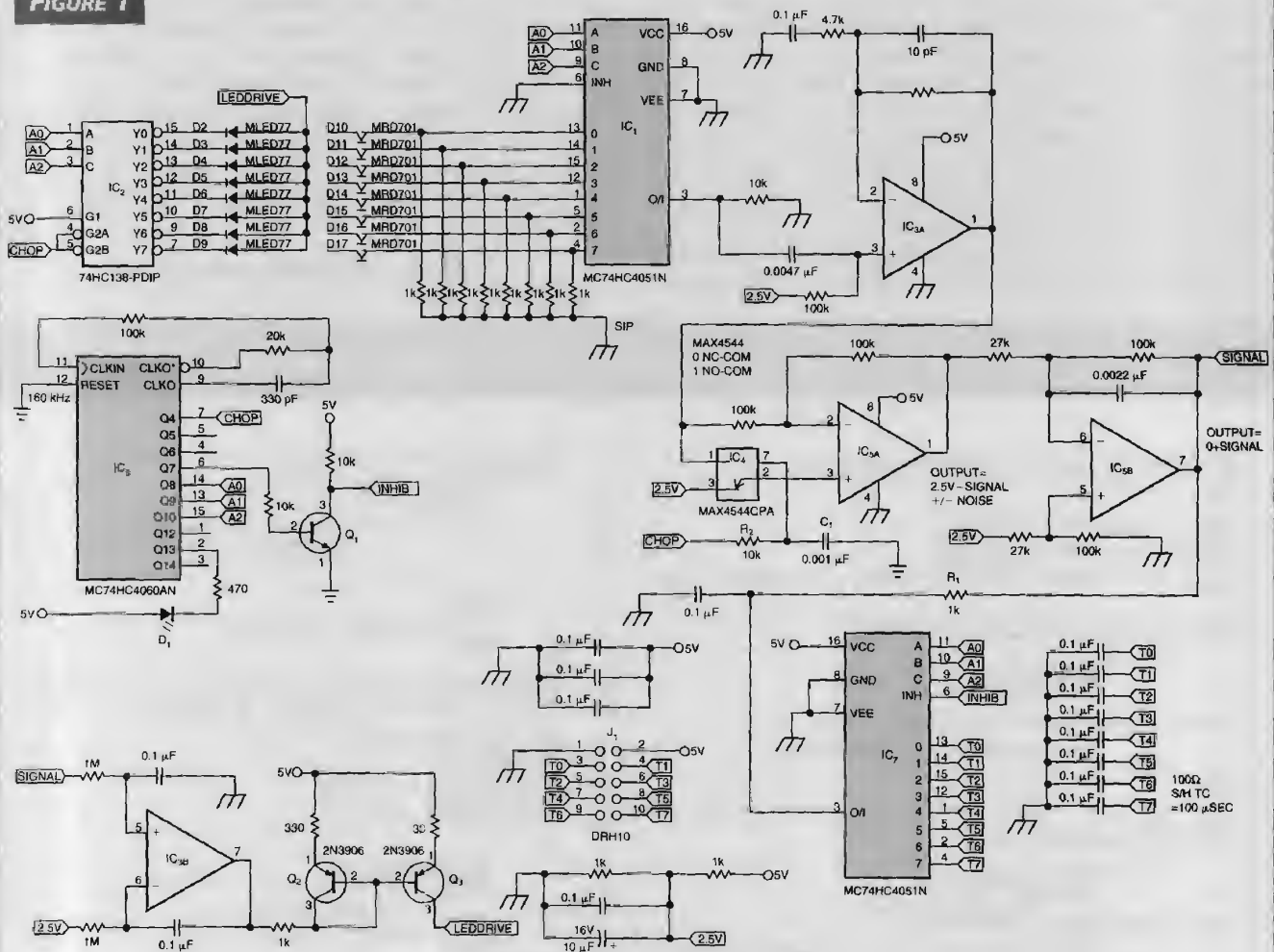
STEVEN SARNS, KESTA TECHNOLOGY INC, WHEAT RIDGE, CO

A project required building a synchronous-demodulator circuit to track a line drawn on paper. The beauty of the synchronous-modulator/demodulator approach is its inherent noise rejection. The method rejects nearly all out-of-band noise, whether from internal drift or external illumination. This rejection is a boon in optical tracking, where the return signal is inevitably buried in 120-Hz ambient light, amplifier offsets, and temperature drifts. The circuit in Figure 1 is inexpensive, and it operates from 5V dc. The circuit scans eight LED/sensor pairs every 22 msec and stores the result in eight sample/hold (S/H) capacitors for interrogation by a  $\mu$ P-driven

ADC. The purpose of the circuit is to determine which sensor is above the line.

The 74HC4060 generates a chopper signal at a rate of 3 kHz. Every eight chopper cycles, the circuit increments the three address lines, thereby selecting the LED to illuminate through the 74HC138 multiplexer. The chopper signal gates the 138 on and off, thus producing the synchronous modulation of the signal at the selected LED. A 74HC051 demultiplexes the received signal from the sensor array, using the three address lines. A 2.5V rail is the signal reference for the next two stages of amplification to produce maximum signal

FIGURE 1



Synchronous modulation and demodulation yield an optical line tracker with high immunity to ambient-light noise and temperature and component drifts.

swing. The signal ac-couples to a gain stage, set nominally at a gain of 20. Two poles of lowpass filtering provide first-order 120-Hz rejection.

The next amplifier switches between gains of 1 and -1. This switching is the heart of the synchronous demodulator. If no noise were present with the incoming signal, the output would appear as a dc level equal to one-half the incoming peak-to-peak signal. The circuit asynchronously amplifies any noise appearing on the incoming signal, such that the output of the demodulator swings above and below the expected dc level by the amount of the noise. The next stage of amplification averages out this noise signal. The third stage of amplification averages the demodulator's output and references the result to ground, such that an increasing return signal produces an increasing output.

A gain of four allows the output signal to approach 4V, while still providing the demodulator stage enough overhead to reject noise. The signal multiplexes onto eight S/H capacitors, using another 74HC4051 and the three address lines. Resistor  $R_1$  prevents third-stage oscillation by isolating the amplifier from the S/H capacitors. The circuit limits the actual sample period to the last four chopper cycles to allow the demodulator to settle after changing channels. A portion of the signal, lowpass-filtered and buffered, drives the 10-to-1 current mirror ( $Q_1$ ,  $Q_2$ ) to establish the drive current to the LEDs. This arrangement results in a constant average output signal of 2.5V over a range of distances from 0.05 to 0.5 in.

The signal from the sensors undergoes a delay because of the relatively slow photodetectors. Therefore, the chopper

signal must also have a delay (via  $R_2C_1$ ) before controlling the  $\pm 1$  gain switch, so the phase matches as closely as possible. Select the appropriate delay to minimize the carrier-frequency noise on the output signal. You can use low-cost components throughout. Suitable choices include an LM358AN for  $IC_3$  and a CA3260 for  $IC_5$ . You should use CMOS op amps because of the high resistance values in the circuit. The second stage should have rail-to-rail output capability to reject noise effectively. Amplifier saturation appears on the output as noise.

Amplifier speed is not of great concern, because the phototransistors are the slowest components in the processing path. Individual sensors vary from unit to unit. You can select the eight emitter resistors to produce matching outputs, if desired. You can place the eight LEDs along the edge of the pc board on the solder side, and the eight sensors on the component side, spaced 0.2 in. apart. Using visible-light LEDs, a line drawn by a "Sharpie" marker approximately 30 mils wide results in a 50% reduction of the signal of the channel directly over the line at a 1-in. distance. A number-2 pencil line results in a 5% signal reduction at a 0.25-in. distance. The higher output of infrared LEDs would further improve the performance. Listing 1 gives the Basic source code for the tracker operation. You can download the routine from EDN's Web site, [www.ednmag.com](http://www.ednmag.com). At the registered-user area, go into the Software Center to download the files from DI-SIG, #2211, (DI #2211)



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## LISTING 1-BASIC SOURCE CODE FOR OPTICAL TRACKER

```
REM Follow line - program demonstrates line tracker
REM print sensor number that line is currently under
REM 02/9/98
```

```
CONST CRLF AS STRING = "\013\010"
DECLARE baseline AS LONG ARRAY
DECLARE sensor_output AS LONG ARRAY
DECLARE deviation AS LONG ARRAY
GLOBAL index AS INTEGER, channel AS INTEGER, n AS INTEGER, lost AS INTEGER
```

```
REM sensor array calibration must be done while not over a line
```

```
SUBROUTINE calibrate_sensor_array()
    n = 100
    FOR channel = 0 TO 7
        baseline[channel] = 0
        FOR index = 1 TO n
            baseline[channel] = baseline[channel] + AIN(channel)
        NEXT
    NEXT
    baseline[channel] = baseline[channel] / n
END
```

```
REM read all input channels into array, calc deviation of each channel
```

```
from baseline
SUBROUTINE read_sensor_array()
    n = 10
    FOR channel = 0 TO 7
        sensor_output[channel] = 0
        FOR index = 1 TO n
            sensor_output[channel] = sensor_output[channel] + AIN(channel)
        NEXT
        sensor_output[channel] = sensor_output[channel] / n
        baseline[channel]
        REM deviation will be expressed as percent
        deviation[channel] = ABS((sensor_output[channel] * 100) / baseline[channel])
    NEXT
END
```

```
REM find the channel with maximum deviation from baseline
FUNCTION find_line() AS INTEGER
    LOCAL max_deviation AS LONG, best_guess AS INTEGER
    find_line = -1
    FOR channel = 0 TO 7
        IF deviation[channel] > max_deviation
            max_deviation = deviation[channel]
            best_guess = channel
        ENDIF
    NEXT
    IF max_deviation > 15
        find_line = best_guess
    ENDIF
END
```

```
SUBROUTINE AIN_CONFIG(vmode AS INTEGER, value AS INTEGER):49
FUNCTION AIN(channel AS INTEGER) AS INTEGER:48
```

```
REM ***** main routine *****
PRINT CRLF, "Start", CRLF
AIN_CONFIG(0,1)
DIM baseline[8] AS LONG
DIM sensor_output[8] AS LONG
DIM deviation[8] AS LONG
calibrate_sensor_array()
```

```
DO
    read_sensor_array()
    channel = find_line()
    IF channel > -1
        PRINT CRLF, channel
    ELSE
        PRINT CRLF, "Lost"
    ENDIF
LOOP UNTIL 0
```

# $\mu$ C implements pushbutton light dimmer

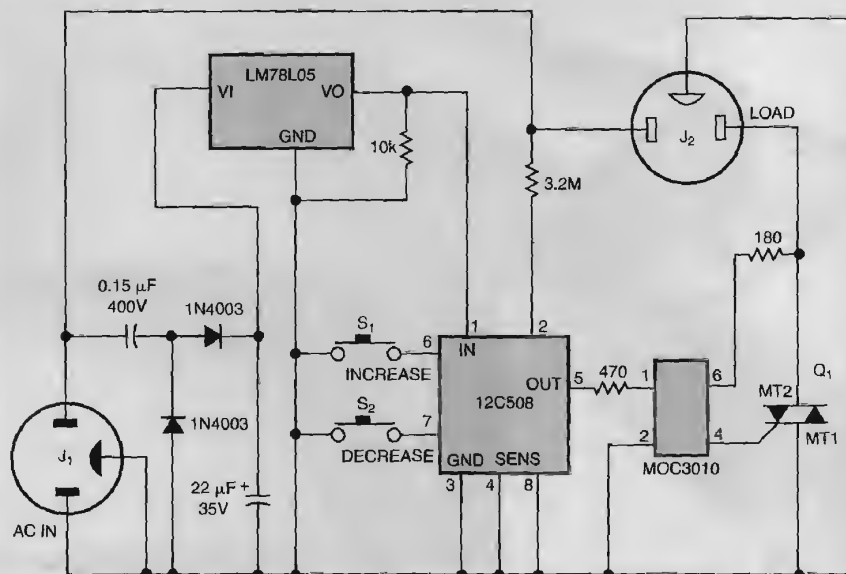
WILLIAM GRILL, RIVERHEAD SYSTEMS, LITTLETON, CO

Using a 12C508 Microchip  $\mu$ C, as described in the *EDN*, Dec 18, 1997, Design Idea, "Controller provides multimode phase control," you can implement an inexpensive dimmer control to provide constant-power control of a line-powered load (Figure 1). The previously described controller evaluated an input frequency relative to its local time reference and scaled a tabled phase offset to define the specific phase-step timing relative to the zero crossings of the monitored input. A two-button, debounced counter provided manual indexing of the tabled offset. The table used  $5^\circ$  steps. Redefinition of the table allowed nonlinear phase indexing to accommodate specific requirements, including constant power or luminescence profiles. The code, usable from 1 Hz to 1 kHz, accommodated common 60-Hz line-power applications, such as the one described here.

You can connect the 12C508 controller in Figure 1 directly to the ac line by limiting the line pin's input current to a few microamperes. The combination of the 3.2-M $\Omega$  resistor and the use of the  $\mu$ C's internal diode in pin 2 allows monitoring the ac line with only a small phase error. A simple power converter and an inexpensive LM78L05 linear regulator provide the  $V_{DD}$  supply to the  $\mu$ C directly from the ac power line. With the controller-mode and sense pins 3 and 4 grounded, the processed output pulse couples directly to the triac,  $Q_1$ , using an optically coupled MOC3010 diac. In Figure 2a, the typical output waveform references to MT2 of the triac. This application modifies the phase table to provide a 78-step index, calculated to provide constant power. Thus, the areas under the curve are approximately the same for all steps (Figure 2b). You can download the  $\mu$ C code for this application from *EDN*'s Web site, [www.ednmag.com](http://www.ednmag.com). At the registered-user area, go into the Software Center to download the files from DI-SIG, #2212. (DI #2212)

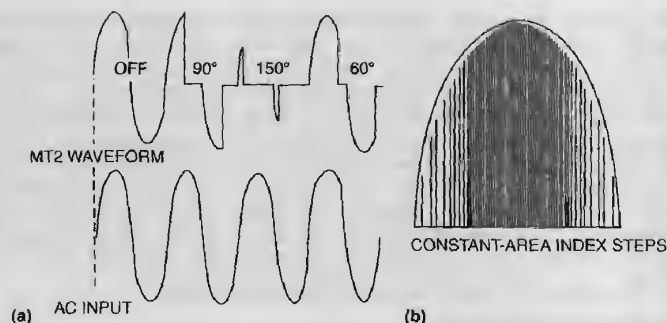
EDN

FIGURE 1



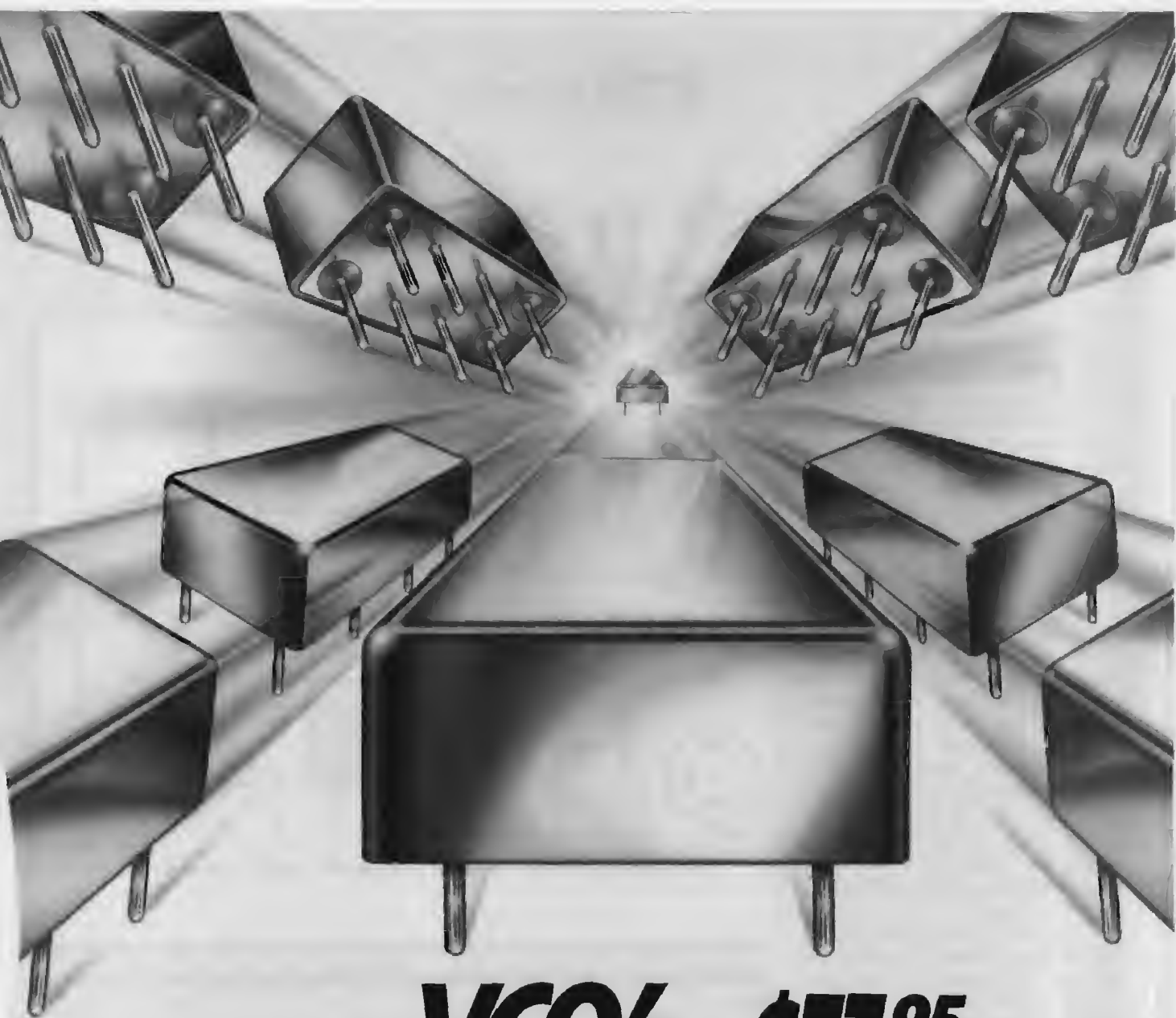
This inexpensive,  $\mu$ C-controlled pushbutton light dimmer operates directly from the ac line.

FIGURE 2



The  $\mu$ C in Figure 1 controls a diac/triac combination to provide phase control (a) in a light-dimming application. A 78-step index in the phase table provides constant-power steps (b).

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K-POS3 \$79.95 (Contains 2ea. POS-1060, -1400, -2000).

Model	Freq. Range (MHz)	Phase Noise (dBc/Hz) SSB @10kHz Typ.	Harmonics (dBc) Typ.	Current (mA) @ +12V DC Max.	Price (Qty.5-49) \$ ea.
NEW POS-25	15-25	-105	-26	20	16.95
POS-50	25-50	-110	-19	20	11.95
POS-75	37.5-75	-110	-27	20	11.95
POS-100	50-100	-107	-23	20	11.95
POS-150	75-150	-103	-23	20	11.95
POS-200	100-200	-102	-24	20	11.95
POS-300	150-280	-100	-30	20	13.95
POS-400	200-380	-98	-28	20	13.95
POS-535	300-525	-93	-26	20	13.95
POS-765	485-765	-85	-21	22	14.95
NEW POS-900W	500-900	-85	-26	25	16.95
NEW POS-1000W	500-1000	-83	-26	20	16.95
POS-1025	685-1025	-84	-23	22	16.95
POS-1060	750-1060	-80	-11	30*	14.95
POS-1400	975-1400	-85	-11	30*	14.95
POS-2000	1370-2000	-95	-11	30*	14.95

\*Max. Current (mA) @ 8V DC.

Notes: Tuning voltage 1 to 16V required to cover freq. range. 1 to 11V for POS-25, 1 to 20V for POS-1060 to -2000. 3dB modulation bandwidth for POS-25 is 60kHz, POS-50 to -1025 is 100kHz, and POS-1060 to -2000 is 1MHz (all typ). Operating temperature range: -55°C to +85°C. 5V tuning models available. Consult RF/IF Designer's Guide or call Mini-Circuits.

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# Charger selects between full and trickle charge

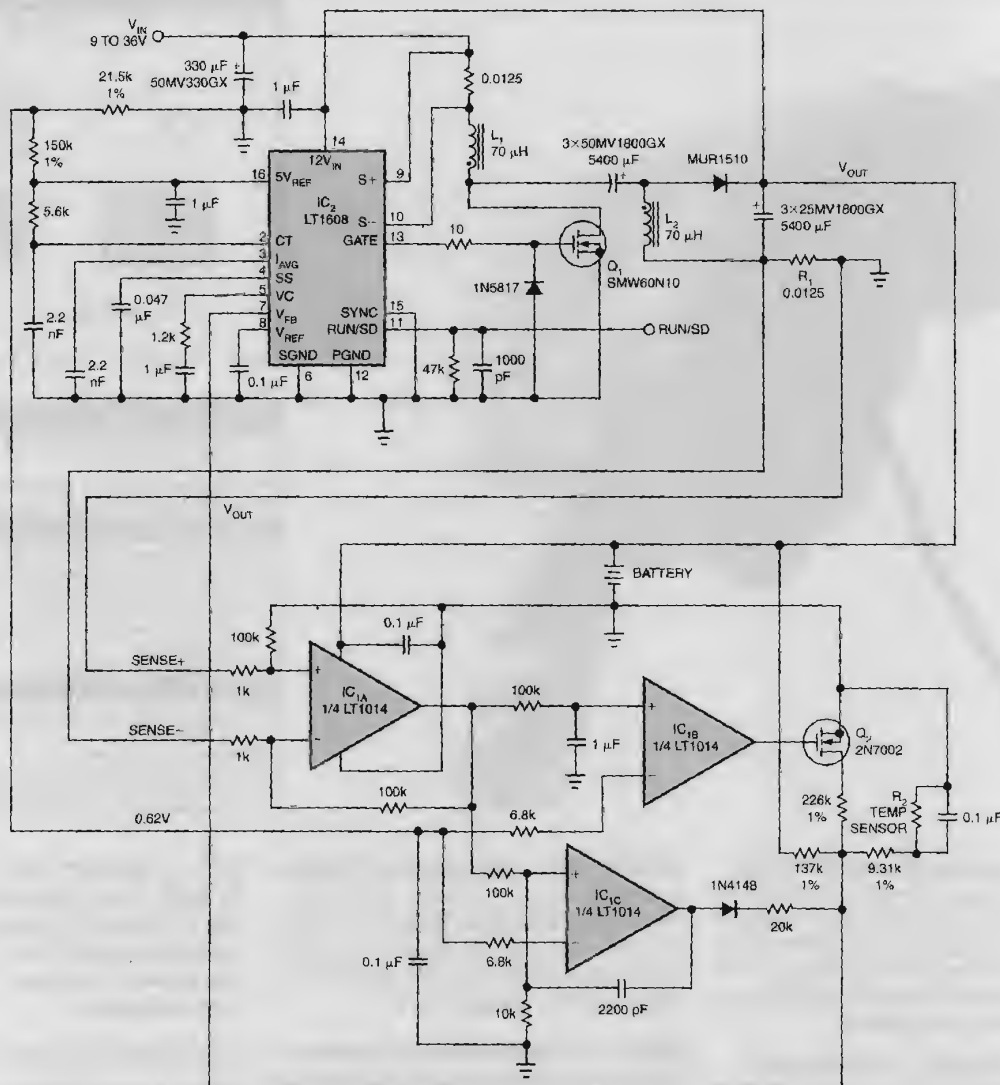
AJMAL GODIL, LINEAR TECHNOLOGY CORP, MILPITAS, CA

The circuit in Figure 1 charges a lead-acid battery at full charge voltage while monitoring the charge current. When the charge current decays to approximately  $0.1C$ , where  $C$  is the capacity of the battery, the charger automatically switches to a lower trickle-charge voltage. The battery can remain in this state for a long time, minimizing any degradation of battery life.

The most common method for charging sealed lead-acid

batteries is constant-voltage charging, which means that the charger voltage is uniform, regardless of the state of the battery. When the battery is fully discharged, its voltage is less than the charge voltage and the current flow into the battery is large. As the battery charges, its voltage increases, and the charge current decreases. Although the current of a constant-voltage charger starts out high, it decays exponentially. Because of this exponential decay, you can potentially over-

FIGURE 1



**NOTES:**

Q<sub>1</sub> AND D<sub>1</sub> NEED HEAT SINKS.

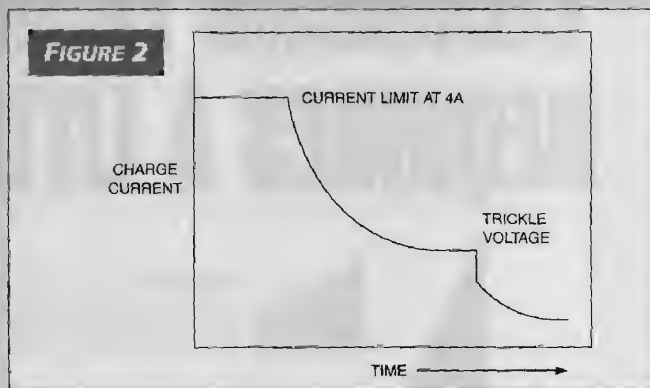
L<sub>1</sub> AND L<sub>2</sub> = COILTRONICS CTX01-14002.

This sealed lead-acid-battery charger monitors the charge current and switches to a trickle-charge voltage of 16.45V when the charge current drops below 0.5A.

charge the battery using a fast-charging scheme. However, the charger in Figure 1 avoids overcharging by always monitoring the charge current.

The 75W sealed lead-acid battery charger for seven tall D cells in Figure 1 uses a high-power, current-mode switching regulator ( $IC_2$ ). The required full-charge voltage is 2.45V/cell, and the trickle-charge voltage is 2.35V/cell. Discharged batteries can draw as much as 16A of charge current because they have low internal resistance. The charger circuit is current-limited at 4A. This current limit is equivalent to 1C, which is the maximum current into the battery and the charger's safe limit.

When you plug a discharged battery into the charger, the battery attempts to draw as much as 16A. Because the charger is current-limited, it delivers only about 4A, and the battery voltage starts rising. When the charge current drops below 4A,  $IC_2$ 's internal feedback loop takes over and regulates to a charging voltage of 17.15V. As the battery charges, it draws less and less charge current (Figure 2). When the charge current decays to 0.5A (0.125C), it produces a voltage drop of 6.25 mV across  $R_1$ .  $IC_{1A}$  amplifies this voltage by 100, which trips comparator  $IC_{1B}$  and turns off  $Q_2$ . This action lowers the feedback resistance and sets the lower trickle-charge voltage to 16.45V. The charge current continues to fall as the battery charges. Additionally, the circuit automatically



**When first charging a fully discharged battery, the charger delivers 4A, which is the current limit. As the battery continues to charge, the charge current decays exponentially. When the charge current falls to 0.5A, the charger switches to a trickle charge**

adjusts the charge voltage as a function of temperature by using  $R_2$ , a silicon temperature sensor, to give a  $-3 \text{ mV}/^\circ\text{C}$  temperature coefficient. (DI #2203)

EDN

**To Vote For This Design, Circle No. 467**

## Power supply runs off battery or wall adapter

DAVID BELL, LINEAR TECHNOLOGY CORP, MILPITAS, CA

Most portable products need to operate from both a battery and an external wall adapter. Although conceptually simple, implementing a robust and bulletproof design that properly switches between these two power sources can be challenging. The circuit in Figure 1a delivers 5V at 50 mA from four AAA alkaline cells or from a 6V wall adapter, which is enough power for many handheld applications. This circuit meets the following design criteria:

- Step-up/step-down dc/dc conversion: Delivering 5V from four alkaline cells—a range of 6.2 to 3.2V—or from a 6V wall adapter means that the converter must be capable of stepping up or down to deliver a regulated 5V output.
- Reverse-battery protection: When using individual batteries, the power supply should be able to tolerate reverse-battery insertion. This circuit is undamaged, even when someone installs all four cells backward.
- Reverse-wall-adapter protection: Wall adapters come in many flavors and both connector polarities. As with reverse batteries, reversing the voltage applied to the wall-adapter input does not damage this power supply.
- Battery operation to 100% discharge: Alkaline batteries deliver their rated capacity only if they discharge all the way down to 0.8V/cell. This power supply can deliver full-rated current to as low as 0.8V/cell, with four alkaline cells in series.
- Battery reverse-current prevention: Reverse charging cur-

rent can result in electrolyte leakage from normal alkaline cells. The design must never allow reverse battery current to flow when the wall adapter is connected.

- Very low battery current drain when off: The design must minimize off-state current drain to sustain battery capacity when the product is off. This circuit draws only 25  $\mu\text{A}$  when shut down, which is only slightly more than a AAA battery's self-discharge current.
- Clean switch-over between battery and wall adapter: Many products, even some expensive notebook computers, momentarily lose regulation when switching between a battery and a wall adapter. This power supply maintains output regulation when you insert or remove the wall adapter and operates from the wall adapter without batteries installed.
- Battery-drain prevention even with an inserted wall adapter: Surprising as this fact may seem, some products continue to drain the battery if the wall-adapter voltage is slightly less than the battery voltage, which is possible with fresh cells. This circuit operates from the wall adapter if its voltage is greater than 4.5V, even if the battery voltage is higher.

The heart of the circuit is  $IC_1$ , a charge-pump dc/dc converter. This converter is capable of step-up or -down operation over a 3.2 to 10V input range. The IC uses no inductors and requires only one external charge-pump capacitor for





# Four ICs implement video AGC and dc restore

TAMARA AHRENS AND MIKE WONG, ELANTEC SEMICONDUCTOR INC, MILPITAS, CA

Four ICs—a multiplier, a sync separator, an op amp, and a dc-restore IC—along with a handful of passive components can implement a complete AGC and dc-restore circuit for video signals (Figure 1). The circuit consists of three main paths: the signal path, the gain-control path, and the dc-restore path. The input video signal first passes through an attenuator so that the circuit can handle oversized voltages. The attenuated signal drives IC<sub>1</sub>, which multiplies this signal by the gain-control voltage. Both the gain-control and the dc-restore path use the output of the multiplier.

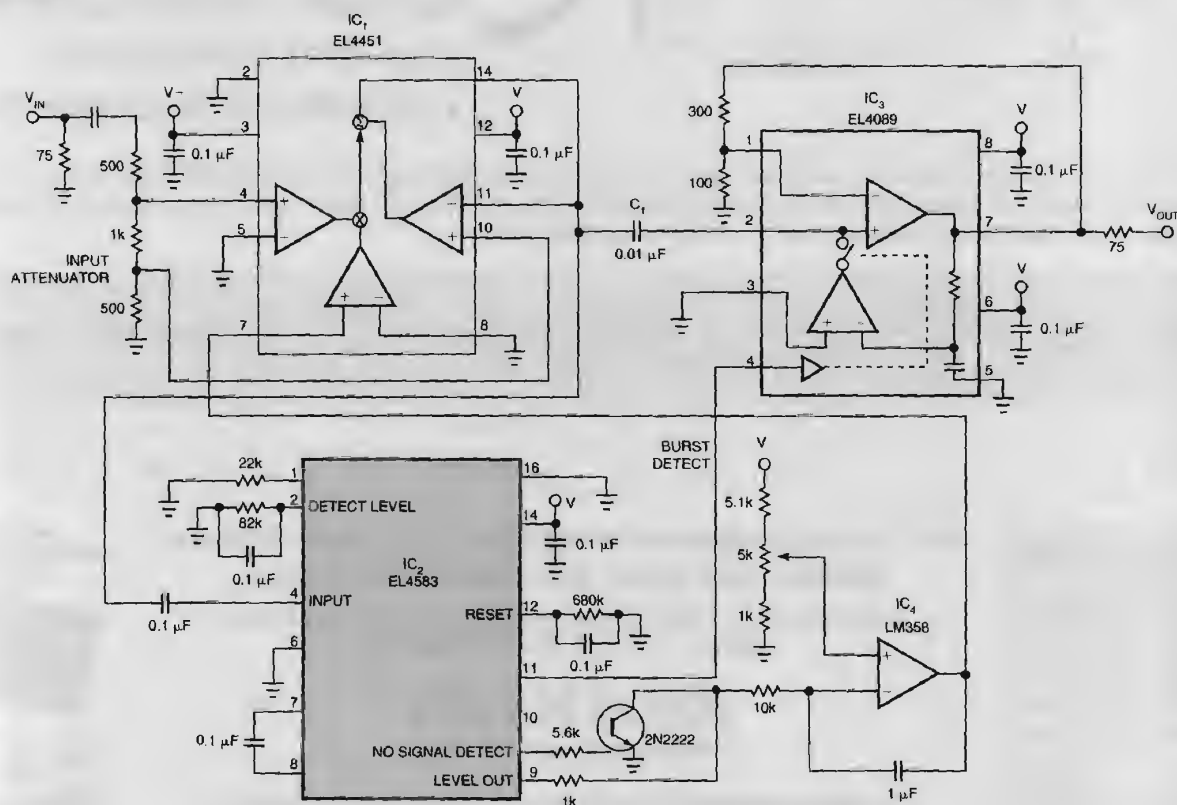
IC<sub>2</sub>'s sync separator recovers the timing-logic outputs of the video signal and also provides a level-out signal. This signal corresponds to twice the tip-to-porch voltage that the gain servo op-amp, IC<sub>4</sub>, compares with a reference voltage of 0.7V, which is nominal for the NTSC standard. The integrated output of IC<sub>4</sub> drives the second input of multiplier IC<sub>1</sub>. You

can adjust the potentiometer for proper peak-to-peak amplitude through this servo system. In the event of a loss of signal, which pin 10 of the sync separator indicates, an npn transistor turns on, shunting the op amp's input to ground and sending the V<sub>GAIN</sub> control signal to its maximum setting.

IC<sub>2</sub> also provides the dc-restore signal. The burst-detect output informs IC<sub>3</sub>'s dc-restore IC when to hold the previous value and when to restore the current output voltages. When the burst-detect signal is logic 1, the circuit stores the offset voltage on coupling capacitor C<sub>1</sub>. Conversely, when a logic 0 appears at pin 4 of IC<sub>3</sub>, the dc offset is null. You can reduce the value of C<sub>1</sub> to allow for compensation of larger correction voltages at the cost of greater droop during the hold time. IC<sub>3</sub> also contains an amplifier capable of driving back-terminated 75Ω cable.

Two passive components associated with IC<sub>2</sub> are critical.

FIGURE 1



This complete AGC and dc-restore circuit for video signals comprises a signal path, a gain-control path, and a dc-restore path.



The resistance on pin 2 determines the minimum signal level that the circuit can detect. A value of 82 k $\Omega$  allows IC<sub>2</sub> to detect signals greater than 100 mV at the sync tip. The other critical value is RESET at pin 12. This resistor sets the reference current and, subsequently, all the internal timing func-

tions, for the entire chip. For NTSC video with a 15.7-kHz scan rate, a value of 681 k $\Omega$  with 1% tolerance is necessary. (DI #2221) **EDN**

To Vote For This Design, Circle No. 469

## "Useless" masked $\mu$ Cs make useful PC peripherals

ALEC BATH, MOTOROLA INC, NORTHBROOK, IL

A software bug or a new code revision can often render hundreds of masked  $\mu$ Cs all but useless for production purposes. However, by tapping into the 68HC11's bootstrap mode, you can attach these  $\mu$ Cs to a PC's RS-232C serial port and put them to work. In the MC68HC11E9, 512 bytes of RAM are available for downloading a user's program. 512 bytes of EEPROM are also available to the programmer, as well as an 8-bit ADC, two serial ports, various timer functions, and many I/O ports. The masked-ROM locations are unused.

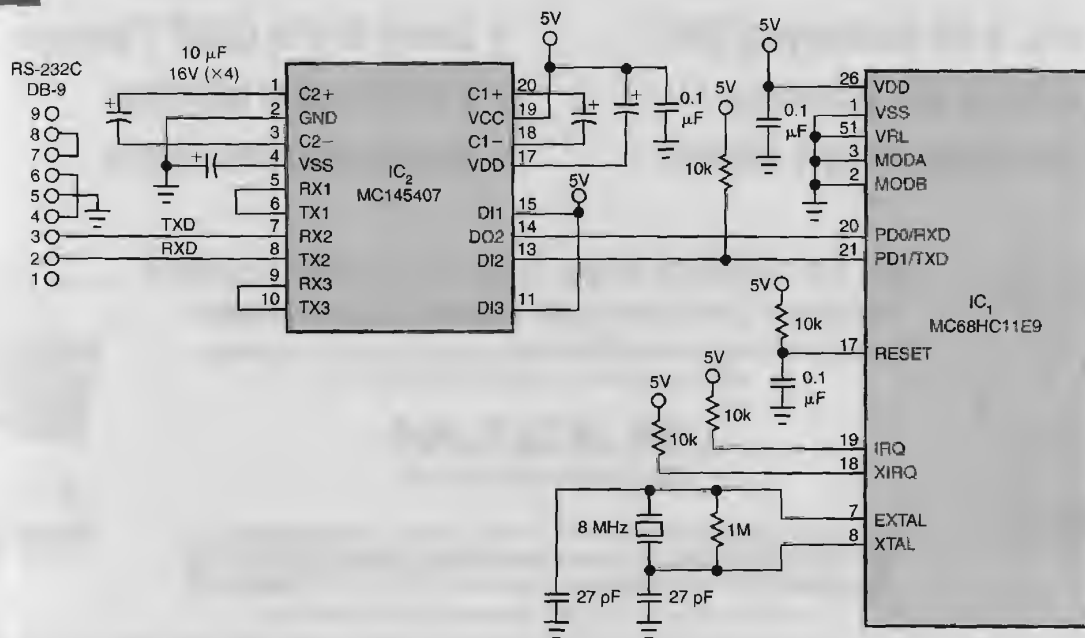
Figure 1 shows the connection from a 68HC11E9 (IC<sub>1</sub>) to a PC's eight-pin RS-232C serial port. The HC11 resets into bootstrap mode, and a QuickBasic program downloads an S-record file at 1200 baud. Upon receipt of the final byte, the program executes at the start of RAM. IC<sub>2</sub> is a 5V-only RS-232C level converter. For proper communication synchronization, an 8-MHz crystal is necessary, although other crys-

tal/baud-rate combinations are possible.

The QuickBasic program "bootload.bas" loads an assembled S-record file and strips the header, footer, and checksum information. The program then converts the ASCII text into raw hexadecimal data, adds a preamble \$FF character for communications synchronization, and transmits the data at 1200 baud out COM port 1. The HC11's internal boot-loader-ROM program configures its SCI asynchronous serial port, looks for an \$FF character, and downloads a program in RAM, starting at \$0000. You can download the bootload.bas program from EDN's Web site, [www.ednmag.com](http://www.ednmag.com). At the registered-user area, go into the Software Center to download the file from DI-SIG, #2222. (DI #2222) **EDN**

To Vote For This Design, Circle No. 470

FIGURE 1



By tapping into IC<sub>1</sub>'s bootstrap mode, you can attach the  $\mu$ C to a PC's RS-232C serial port and put the masked  $\mu$ C to work.

# Use a printer port to record digital waveforms

DEAN SHEN, DYCAM INC, CHATSWORTH, CA

To record or capture special waveforms, those that appear once or have no fixed frequency, the usual technique is to use a logic analyzer or a storage oscilloscope. However, these tools are very expensive. Moreover, because of limited memory, a storage scope can record fewer than 1000 samples. The technique presented here provides an alternative method to recording digital waveforms. The idea is to use the PC's printer port to sample waveforms, and the PC's memory to store

data. The large memory capacity of PCs allows you to store large samples. For example, 60 kbytes of memory can store  $8 \times 60,000 = 480,000$  samples.

To sample data as fast as possible and to equalize sample periods, you use Debug directly to write an assembly program to implement the sampling procedure. Once the PC's memory stores the data, it is easy to display the waveform or to save it in a file. You use QBasic to display the waveform. To

## LISTING 1—QBASIC ROUTINE FOR DISPLAYING WAVEFORMS

```
'72 is Up Scan Code
KEY 20, CHR$(0) + CHR$(72)
'73 is UpPg Scan Code
KEY 15, CHR$(0) + CHR$(73)
'80 is Down Scan Code
KEY 21, CHR$(0) + CHR$(80)
'81 is DnPg Scan Code
KEY 16, CHR$(0) + CHR$(81)
'75 is Left Scan Code
KEY 22, CHR$(0) + CHR$(75)
'77 is Right Scan Code
KEY 23, CHR$(0) + CHR$(77)
'1 is ESC Scan Code
KEY 17, CHR$(0) + CHR$(1)

ON KEY(15) GOSUB UpPage
ON KEY(16) GOSUB DownPage
ON KEY(20) GOSUB UpLine
ON KEY(21) GOSUB DownLine
ON KEY(22) GOSUB Left
ON KEY(23) GOSUB Right
ON KEY(17) GOSUB Finish

SCREEN 12
DEF SEG = &H40
DEF SEG = PEEK(&HFE) + 256 * PEEK(&HFF)
LINE (0, 4) - (639, 4)
FOR i% = 0 TO 32
  j% = i% * 19.5
  LINE (j%, 4) - (j%, 0)
NEXT i%

h% = 20
addr0% = &H180
fl% = 0
KEY(17) ON
WHILE fl% = 0

KEY(15) ON
KEY(16) ON
KEY(20) ON
KEY(21) ON
KEY(22) ON
KEY(23) ON

LOCATE 1, 40
PRINT (addr0% - &H180) / 80;
FOR i% = 0 TO 255
  FOR j% = 0 TO 128
    NEXT j%
  NEXT i%

KEY(15) STOP
KEY(16) STOP
KEY(20) STOP
KEY(21) STOP
KEY(22) STOP
KEY(23) STOP

FOR i% = 0 TO 14
  y% = i% * 30 + 20
  addr% = addr0% + 80 * i%
  FOR j% = 0 TO 79
    x% = j% * 8
    SELECT CASE PEEK(addr% + j%)
      CASE 0
        IF j% > 0 THEN
          LINE -(x% - 1, y% + h%)
        END IF
        LINE (x%, y% + h%) - (x% + 7, y% + h%)
      CASE &HFF
        IF j% > 0 THEN
          LINE -(x% - 1, y%)
        END IF
        LINE (x%, y%) - (x% + 7, y%)
      CASE 1
        IF j% > 0 THEN
          LINE -(x% - 1, y% + h%)
        END IF
        LINE (x%, y% + h%) - (x% + 7, y% + h%)
      CASE 3
        IF j% > 0 THEN
          LINE -(x% - 1, y% + h%)
        END IF
        LINE (x%, y% + h%) - (x% + 6, y% + h%)
        LINE (x% + 6, y% + h%) - (x% + 6, y%)
        LINE -(x% + 7, y%)
      CASE 7
        LINE (x%, y% + h%) - (x% + 5, y% + h%)
        LINE (x% + 5, y% + h%) - (x% + 5, y%)
        LINE -(x% + 7, y%)
      CASE &HFF
        LINE (x%, y% + h%) - (x% + 4, y% + h%)
        LINE (x% + 4, y% + h%) - (x% + 4, y%)
        LINE -(x% + 7, y%)
      CASE &H1F
        LINE (x%, y% + h%) - (x% + 3, y% + h%)
        LINE (x% + 3, y% + h%) - (x% + 3, y%)
        LINE -(x% + 7, y%)
      CASE &H3F
        LINE (x%, y% + h%) - (x% + 2, y% + h%)
        LINE (x% + 2, y% + h%) - (x% + 2, y%)
        LINE -(x% + 7, y%)
      CASE &H7F
        LINE (x%, y% + h%) - (x% + 1, y% + h%)
        LINE (x% + 1, y% + h%) - (x% + 1, y%)
        LINE -(x% + 7, y%)
      CASE &H80
        IF j% > 0 THEN
          LINE -(x%, y%)
        END IF
        LINE (x%, y%) - (x%, y% + h%)
        LINE -(x% + 7, y% + h%)
      CASE &H81
        IF j% > 0 THEN
          LINE -(x%, y%)
        END IF
        LINE (x%, y%) - (x%, y% + h%)
        LINE -(x% + 5, y% + h%)
        LINE -(x% + 5, y%)
        LINE -(x% + 7, y%)
      CASE &H83
        IF j% > 0 THEN
          LINE -(x%, y%)
        END IF
        LINE (x%, y%) - (x%, y% + h%)
        LINE -(x% + 6, y% + h%)
        LINE -(x% + 6, y%)
        LINE -(x% + 7, y%)
      CASE &H8C
        LINE (x%, y%) - (x% + 1, y%)
        LINE -(x% + 1, y% + h%)
        LINE -(x% + 7, y% + h%)
      CASE &H81
        LINE (x%, y%) - (x% + 1, y%)
        LINE -(x% + 1, y% + h%)
        LINE -(x% + 6, y% + h%)
        LINE -(x% + 6, y%)
        LINE -(x% + 7, y%)
      CASE &H80
        LINE (x%, y%) - (x% + 2, y%)
        LINE -(x% + 2, y% + h%)
        LINE -(x% + 7, y% + h%)
      CASE &H81
        LINE (x%, y%) - (x% + 2, y%)
        LINE -(x% + 2, y% + h%)
        LINE -(x% + 6, y% + h%)
        LINE -(x% + 6, y%)
        LINE -(x% + 7, y%)
      CASE &H80
        LINE (x%, y%) - (x% + 3, y%)
        LINE -(x% + 3, y% + h%)
        LINE -(x% + 7, y% + h%)
    END SELECT
  NEXT j%
NEXT i%
```

compare the recorded waveform and the waveform from a standard signal generator, you calculate the sample period. We have used the method successfully to record many different digital waveforms. Figure 1 shows the sampling circuit. Listing 2 gives the Debug sampling program. After execution, the routine saves the segment of recorded data in 40h:FEh.

The Basic program in Listing 1 can easily access the data. This method uses a Dallas Semiconductor one-wire communications protocol. The PC is a 33-MHz 80486 machine; the sample period is approximately 2.03  $\mu$ sec. The method shown here can record only one channel signal. However,

#### LISTING 1—QBASIC ROUTINE FOR DISPLAYING WAVEFORMS (CONTINUED)

```

CASE &HF8
  LINE (x%, y%) - (x% + 4, y%)
  LINE - (x% + 4, y% + h%)
  LINE - (x% + 7, y% + h%)
CASE &HFC
  LINE (x%, y%) - (x% + 5, y%)
  LINE - (x% + 5, y% + h%)
  LINE - (x% + 7, y% + h%)
CASE &HFE
  LINE (x%, y%) - (x% + 6, y%)
  LINE - (x% + 6, y% + h%)
  LINE - (x% + 7, y% + h%)
CASE ELSE
  LINE (x%, y%) - (x% + 7, y% + h%)
PRINT addr0%
END SELECT
NEXT j%
NEXT i%
WEND

KEY(15) OFF
KEY(16) OFF
KEY(20) OFF
KEY(21) OFF
KEY(22) OFF
KEY(23) OFF
KEY(17) OFF

DEF SEG
END

UpLine:
IF addr0% <= (&H3CE0 * 2) THEN
  CLS 1
  addr0% = addr0% + &H50
END IF
RETURN

DownLine:
IF addr0% > &H180 THEN
  CLS 1
  addr0% = addr0% - &H50
END IF
RETURN

UpPage:
IF addr0% <= (&H3CE0 * 2) THEN
  CLS 1
  addr0% = addr0% + &H460
END IF
RETURN

DownPage:
IF addr0% > &H520 THEN
  CLS 1
  addr0% = addr0% - &H460
END IF
RETURN

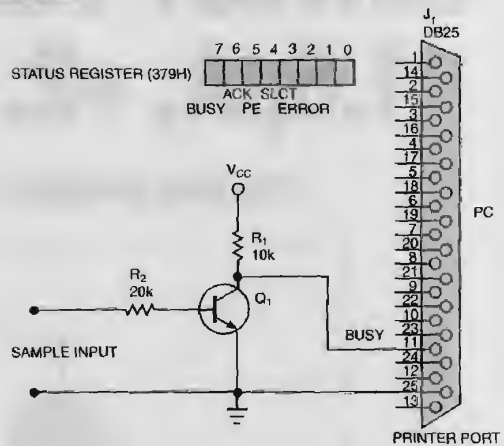
Right:
IF addr0% <= (&H3CE0 * 2) THEN
  CLS 1
  addr0% = addr0% - 1
END IF
RETURN

Left:
IF addr0% > &H180 THEN
  CLS 1
  addr0% = addr0% + 1
END IF
RETURN

Finish:
fl% = 1
RETURN

```

FIGURE 1



This simple circuit allows you to use your PC's printer port to record digital waveforms and to store them in memory.

#### LISTING 2—DEBUG ROUTINE FOR RECORDING WAVEFORMS

```

u100 i3c
1358:0100 BA7903      MOV     DX,0379
1358:0103 EC          IN      AL,DX
1358:0104 2480        AND     AL,80
1358:0106 75FB        JNZ     0103
1358:0108 B900FD      MOV     CX,FD00
1358:0108 BF8001      MOV     DI,0180
1358:010E 51          PUSH    CX
1358:010F B90800      MOV     CX,0008
1358:0112 51          PUSH    CX
1358:0113 EC          IN      AL,DX
1358:0114 90          NOP
1358:0115 90          NOP
1358:0116 D0E0        SHL     AL,1
1358:0118 D0D4        RCL     AH,1
1358:011A 59          POP      CX
1358:011B E21B        LOOP    0138
1358:011D 86E0        XCHG    AH,AL
1358:011F AA          STOSB
1358:0120 59          POP      CX
1358:0121 E2EB        LOOP    010E
1358:0123 8CDB        MOV     BX,DS
1358:0125 B84000      MOV     AX,0040
1358:0128 BEC0        MOV     ES,AX
1358:012A BFF800      MOV     DI,00FE
1358:012D 89D8        MOV     AX,BX
1358:012F AB          STOSB
1358:0130 8EC3        MOV     ES,BX
1358:0132 BA00E0      MOV     DX,E000
1358:0135 CD27        INT     27
1358:0137 90          NOP
1358:0138 90          NOP
1358:0139 90          NOP
1358:013A 90          NOP
1358:013B 90          NOP
1358:013C 90          NOP
1358:013D EB03        JMP     0112

```

you can easily modify the circuit and the sampling program to record two- and four-channel signals. You can download the executable Debug routine and the QBasic source code from EDN's Web site, [www.ednmag.com](http://www.ednmag.com). At the registered-user area, go into the Software Center to download the files from DI-SIG, #2210. (DI #2210)

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